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10/507,408	05/24/2005	Rudi Frenzel	IFX P 2003 NAT 05 WOUS	6890

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EXAMINER	
DILLON, SAMUEL A	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/507,408	FRENZEL ET AL.	
	Examiner	Art Unit	
	Sam Dillon	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-9,12-15,18,20,21 and 23-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-9,12-15,18,20,21 and 23-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. The Examiner acknowledges the applicant's submission of the amendment dated May 7, 2007. Per the amendment, Claims 1, 9 and 15 have been amended.

2. The instant application having Application No. 10/507,408 has a total of 17 claims pending in the application; there are 3 independent claims and 14 dependent claims, all of which are ready for examination by the examiner.

I. RESPONSE TO AMENDMENT(S) / ARGUMENT(S)

3. Applicant's arguments with respect to the 35 U.S.C. 102(b) and 103(a) rejections of the Claims have been fully considered and are **persuasive**, but are moot in view of the new ground(s) of rejection, as described below.

II. REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC ' 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. **Claims 1, 5-9, 12-15, 18, 20, 21 and 23-26** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. **Claim 1** recites the limitation *"each of the plurality of processors simultaneously accessing to any of the blocks"*. It is unclear what the phrasing *"simultaneously accessing to any"* specifically implies, and as such the claim is rendered indefinite. For the purposes of further examination, the Examiner will interpret the claim as implying each of the plurality of processors simultaneously access any of the blocks. Claims 5-8 are rejected by virtue of their dependence.

7. **Claim 9** recites the limitation *"a flow control unit for simultaneously accessing by each of the plurality of processors to any of the blocks"*. It is unclear what is doing the simultaneous accessing and what is being specifically accessed. For the purposes of further examination, the Examiner will interpret the claim as implying the control unit allowing simultaneous access by each of the processors to the blocks. Claims 12-14 are rejected by virtue of their dependence.

8. **Claim 15** recites the limitation *"accessing by each of the plurality of processors to any of the blocks simultaneously"*. It is unclear what is specifically implied by the claim. For the purposes of further examination, the Examiner will interpret the claim as implying each of the plurality of processors simultaneously access any of the blocks. Claims 18, 20, 21 and 23-26 are rejected by virtue of their dependence.

III. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC ' 103 – Gruner and Tran

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. **Claims 1, 5-9 and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gruner et al. *(US Patent Number 3,931,613)* in view of Tran et al. *(US Patent Number 5,809,533)*

11. As per **Claims 1 and 9**, Gruner discloses a method of sharing a memory module *(memory unit, figure 11)* between a plurality of processors *(proc A1 and proc B1, figure 11)* comprising:

dividing the memory module into at least two banks *(column 5 lines 18-23)*, wherein each bank can be accessed by one processor at any one time *(column 4 lines 51-56)*;

dividing each bank in at least one block *(memory words, column 5 lines 36-50)*, wherein each block can be accessed by one of the plurality of processors at any one time *(column 4 lines 51-56)*.

mapping the memory module to allocate sequential addresses to alternate banks of the memory *(column 5 lines 36-50)*; and

storing data bytes in memory *(memory words, column 5 lines 36-50)*, wherein said data bytes at sequential addresses are stored in blocks of alternate banks due to the mapping of the memory;

synchronizing the processors to access different blocks in the banks in response to a detected memory access conflict *(column 2 lines 45-59)*, which is caused by at least two of the processors accessing the same block at the same time *(the conflicting processor is stalled, thus synchronizing the invariant of only one processor accessing a specific bank at the same time, column 13 lines 35-58)*.

Gruner does not disclose each bank being accessible by more than one processor at any one time, and each of the plurality of processors simultaneously accessing to any of the blocks.

Tran discloses each bank being accessible by more than one processor at any one time *(column 2 lines 41-67)*, and each of the plurality of processors simultaneously accessing to any of the blocks *(column 2 lines 41-67)*.

Gruner and Tran are analogous art in that they each deal with multiprocessor memory busses. At the time of the invention, it would have been obvious to a person having ordinary skill in the art to modify Gruner so that it had a dual bus ability to access the memory simultaneously, as taught by Tran. The motivation for doing so would have been to provide an enhanced throughput of data transfer operations between multiple processors and multiple memories *(Tran, column 2l lines 31-38)*. Therefore, it would have been obvious to modify Gruner to have a dual bus setup as per Tran for the benefit of enhanced throughput of data transfer operations, to obtain the invention of Claims 1 and 9.

12. As per **Claim 5**, Gruner and Tran disclose the method of Claim 1 further including

a stop of determining access priorities of the processors when memory access conflict occurs *(Gruner, column 13 lines 16-34)*.

13. As per **Claim 6**, Gruner and Tran disclose the method of Claim 5 wherein the step of determining access priorities comprises

assigning lower access priorities to processors that have caused the memory conflict *(Gruner, inherently implied in column 13 lines 16-34, in that the higher priority processor never causes a conflict because it is assigned the bank whenever it requests it, while a conflict can be caused when the lower priority processor attempts to access the bank when the higher priority processor is using it)*.

14. As per **Claim 7**, Gruner and Tran disclose the method of Claim 5 wherein the step of determining access priorities comprises

assigning lower access priorities to processors that performed a jump *(Gruner, column 13 lines 16-34)*.

15. As per **Claim 8**, Gruner and Tran disclose the method of Claim 8 wherein the step of synchronizing the processors comprises

locking processors with lower priorities for one or more cycles when memory access conflict occurs *(Gruner, column 13 lines 50-58)*.

16. As per **Claim 13**, Gruner and Tran disclose the system of any of Claim 9 wherein

said data bytes comprise program instructions *(Gruner, instruction word, column 5 lines 38-39)*.

Claim Rejections - 35 USC ' 103 – Gruner, Tran and Sakakibara

17. **Claim 12** is rejected under 35 U.S.C. 103(a) as being unpatentable over Gruner et al. *(US Patent Number 3,931,613)* and Tran et al. *(US Patent Number 5,809,533)* as applied above, and further in view of Sakakibara *(US Patent Number 5,857,110)*.

18. As per **Claim 12**, Gruner and Tran disclose the system of Claim 9, but do not disclose a priority register for storing the access priority of each processor.

Sakakibara discloses a priority register for storing an access priority of each processors *(column 11 line 62 to column 12 line 7)*.

Gruner, Tran and Sakakibara are analogous art in that they deal with processor access priorities in multiprocessor systems. At the time of the invention it would have been obvious a person having ordinary skill in the art to combine Gruner and Tran's multiprocessor system with Sakakibara's priority bit register.

The motivation for doing so would have been that having per processor priorities allows raising of the priority of a request issued by a particular processor upon accessing a main storage *(Sakakibara, column 4 lines 55-60)*.

Therefore it would have been obvious to combine Gruner and Tran's multiprocessor system with Sakakibara's priority bit register for the benefit of raising a particular request's priority dynamically, to obtain the invention of Claim 12.

Claim Rejections - 35 USC ' 103 – Gruner, Tran and Handy

19. **Claim 14-15, 18, 20-21 and 23-26** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gruner et al. *(US Patent Number 3,931,613)* and Tran et al. *(US Patent Number 5,809,533)* in view of Handy *("The Cache Memory Book")*

20. As per **Claim 15**, Gruner and Tran disclose a method of sharing a memory module between a plurality of processors comprising:

dividing the memory module in at least two banks *(Gruner, column 5 lines 18-23)*, enabling the memory module to be accessed by more than one processor simultaneously *(Gruner, column 4 lines 51-56 and Tran, column 2 lines 41-67)*;

dividing the banks into at least one block *(Gruner, memory words, column 5 lines 36-50)*, wherein a block can be accessed by one of the plurality of processors at any one time *(Gruner, column 4 lines 51-56)*,

mapping the memory module to allocate sequential addresses to alternate banks of the memory *(Gruner, column 5 lines 36-50)*; and

storing data bytes in the memory module *(Gruner, memory words, column 5 lines 36-50)*, wherein said data bytes in sequential addresses are stored in alternate banks due to the mapping of the memory.

determining whether contention has occurred, wherein two or more processors are accessing the same address range at any one time *(Gruner, column 13 lines 35-58)*;

accessing by each of the plurality of processors to any of the blocks simultaneously *(Tran, column 2 lines 41-67)*.

and synchronizing the processors to access different banks when contention has occurred *(Gruner, the processors are always synchronized to access different banks, column 2 lines 45-59, so when contention occurs the conflicting processor is delayed to preserve the synchronization, column 13 lines 35-58)*.

Gruner and Tran do not disclose providing a first signal path, the first signal path coupling a cache to a processor and the memory module when selected, the cache enabling the processor to fetch a plurality of data words from different banks simultaneously.

Handy discloses providing a first signal path *(data path, page 12 lines 12-14)*, the first signal path coupling a cache *(cache data memory, figure 1.6)* to a processor *(CPU, figure 1.6)* and the memory module when selected, the cache enabling the processor to fetch a plurality of data words from different banks simultaneously *(page 12 lines 3-14)*.

Gruner, Tran and Handy are analogous art in that they both deal with speeding up processor memory accesses. At the time of the invention, it would have been obvious to a person having ordinary skill in the art to modify Gruner and Tran's processor to include a local cache and to grab data from the cache when the cache contains local data, as taught by Handy.

The motivation for doing so would have been that a cache allows a processor to take advantage of temporal and spatial locality by assuring that the repetitive portion of a program executes from a very fast memory while it is being used and resides in slower, less expensive memory when it is waiting to be used *(Handy, section 1.3.2 paragraph 3)*.

Therefore, it would have been obvious to combine Gruner and Tran's multiprocessor memory system with Handy's cache for the benefit of taking advantage of temporal and spatial locality of data to obtain the invention of Claim 15.

21. As per **Claim 14**, Gruner, Tran and Handy disclose the system of any of Claim 9 further comprising a plurality of critical memory modules *(Handy, cache data memory for each processor, figure 1.6)* for storing a plurality of data bytes for each processor for reducing memory access conflicts.

22. As per **Claim 18**, Gruner, Tran and Handy disclose the method of Claim 17 wherein the address range coincides with at least one block *(Gruner, col. 13 lines 35-58)*.

23. As per **Claim 20**, Gruner, Tran and Handy disclose the method of the Claim 15 further including the step of providing a second signal path, the second signal path coupling the processor to the memory module when selected *(Handy, cache miss, page 12 lines 3-14)*.

24. As per **Claim 21**, Gruner, Tran and Handy disclose the method of the Claim 15 further including a step of activating the second signal path when contention has not occurred *(Handy, cache miss, page 12 lines 3-14 and Gruner, col. 13 lines 35-58)*.

25. As per **Claim 23**, Gruner, Tran and Handy disclose the method of the Claim 15 further including a step of determining access priorities of the processors when contention has occurred *(Gruner, column 13 lines 16-34)*.

26. As per **Claim 24**, Gruner, Tran and Handy disclose the method of Claim 23 wherein the step of determining access priorities comprises

assigning lower access priorities to processors that have caused the contention *(inherently implied in Gruner, column 13 lines 16-34, in that the higher priority processor never causes a conflict because it is assigned the bank whenever it requests it, while a conflict can be caused when the lower priority processor attempts to access the bank when the higher priority processor is using it).*

27. As per **Claim 25**, Gruner, Tran and Handy disclose the method of the Claim 19 wherein the step of synchronizing the processors comprises

inserting wait states for processors with lower priorities when contention occurs *(Gruner, column 13 lines 50-58).*

28. As per **Claim 26**, Gruner, Tran and Handy disclose the method of the Claim 15

further including a step of activating the first signal path when contention has occurred *(Handy, page 12 lines 3-14).*

IV. CLOSING COMMENTS

a. STATUS OF CLAIMS IN THE APPLICATION

29. The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. ' 707.07(i):

a(1). CLAIMS NO LONGER IN THE APPLICATION

30. Claims 2-4, 10, 11, 16, 17, 19, 22 and 27-34 stand cancelled by the Applicant's amendments.

a(2). CLAIMS REJECTED IN THE APPLICATION

31. Per the instant office action, Claims 1, 5-9, 12-15, 18, 20, 21 and 23-26 have received an action on the merits and are subject of a non-final action.

b. DIRECTION OF FUTURE CORRESPONDENCES

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Dillon whose telephone number is 571- 272-8010. The examiner can normally be reached on 9:30-6:00.

33. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

IMPORTANT NOTE

34. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SAD

Sam Dillon
Examiner
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